

CLAIMS

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(96)

1. Apparatus for processing data, said apparatus comprising:  
 a data processing register operable to store a data value;  
 5 a register writing circuit operable to store a data value to said data processing register; and  
 three or more further registers; wherein  
 when said register write circuit writes a data value to said data processing register, said register write circuit also writes data values to three or more further  
 10 registers such that a fixed relative number of bits within said data processing register and said three or more further registers as a whole transition from high to low and from low to high irrespective of what data value is being written to said data processing register and what data value was previously stored within said data processing register.
- 15 2. Apparatus as claimed in claim 1, wherein when said register write circuit writes a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value of  $Y_i$ , said register write circuit also writes to corresponding bit positions within three further registers respective values of:  
 20 an inverse of  $X_i$ ;  
 a new value  $Rd_i$  given by  $(\text{inverse}(X_i \text{ XOR } Y_i)) \text{ XOR } (\text{a value of } Rd_i \text{ currently stored})$ ; and  
 an inverse of said new value of  $Rd_i$ .
- 25 3. Apparatus as claimed in any one of claims 1 and 2, wherein said data processing register is one of a plurality of data processing registers of a register bank.
4. Apparatus as claimed in claim 2, wherein said three further registers comprise a dedicated dummy register dedicated to said data processing register and two shared  
 30 dummy registers shared between said plurality of data processing registers of said register bank.
5. Apparatus as claimed in claim 1, wherein when said register write circuit writes a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value  
 35 of  $Y_i$ , said register write circuit also writes to corresponding bit positions within three

further registers comprising a dedicated dummy register dedicated to said data processing register and two shared dummy registers shared between said plurality of data processing registers of said register bank such that said dedicated dummy register stores said inverse of  $X_i$  and said two shared dummy registers store said exclusive logical OR of  $X_i$  with  $Y_i$  and said inverse of the exclusive logical OR of  $X_i$  with  $Y_i$ .

6. Apparatus as claimed in any one of claims 4 and 5, wherein said three further registers are provided for a subset of said plurality of data processing registers of said register bank.

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7. A method of processing data, said method comprising the steps of:

storing a data value in a data processing register; and

when said data value is stored in said data processing register also storing data values within three or more further registers such than a fixed relative number of bits within said data processing register and said three or more further registers as a whole transition from high to low and from low to high irrespective of what said data value is being written to data processing register and what data value was previously stored within said data processing register.

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8. A method as claimed in claim 7, wherein when writing a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value of  $Y_i$ , also writing to corresponding bit positions within three further registers respective values of:

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an inverse of  $X_i$ ;

a new value  $Rd_i$  given by  $(\text{inverse}(X_i \text{ XOR } Y_i)) \text{ XOR } (\text{a value of } Rd_i \text{ currently stored});$  and

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an inverse of said new value of  $Rd_i$ .

9. A method as claimed in any one of claims 7 and 8, wherein said data processing register is one of a plurality of data processing registers of a register bank.

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10. A method as claimed in claim 8, wherein said three further registers comprise a dedicated dummy register dedicated to said data processing register and two shared dummy registers shared between said plurality of data processing registers of said register bank.

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11. A method as claimed in claim 7, wherein when writing a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value of  $Y_i$ , also writing to corresponding bit positions within three further registers comprising a dedicated dummy register dedicated to said data processing register and two shared dummy registers shared between said plurality of data processing registers of said register bank such that said dedicated dummy register stores said inverse of  $X_i$  and said two shared dummy registers store said exclusive logical OR of  $X_i$  with  $Y_i$  and said inverse of the exclusive logical OR of  $X_i$  with  $Y_i$ .
- 10 12. A method as claimed in any one of claims 10 and 11, wherein said three further registers are provided for a subset of said plurality of data processing registers of said register bank.

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(78)

1. Apparatus for processing data, said apparatus comprising:

a data processing register operable to store a data value;

5 a register writing circuit operable to store a data value to said data processing register; and

three or more further registers; wherein

when said register write circuit writes a data value to said data processing register, said register write circuit also writes data values to three or more further registers such that a fixed relative number of bits within said data processing register and said three or more further registers as a whole transition from high to low and from low to high irrespective of what data value is being written to said data processing register and what data value was previously stored within said data processing register.

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2. Apparatus as claimed in claim 1, wherein when said register writing circuit writes a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value of  $Y_i$ , said register writing circuit also writes to corresponding bit positions within three further registers respective values of:

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an inverse of  $X_i$ ;

a new value  $Rd_i$  given by  $(\text{inverse}(X_i \text{ XOR } Y_i)) \text{ XOR } (\text{a value of } Rd_i \text{ currently stored});$  and

an inverse of said new value of  $Rd_i$ .

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3. Apparatus as claimed in any one of claims 1 and 2, wherein said data processing register is one of a plurality of data processing registers of a register bank.

4. Apparatus as claimed in claim 2, wherein said three further registers comprise a dedicated dummy register dedicated to said data processing register and two shared dummy registers shared between said plurality of data processing registers of said register bank.

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5. Apparatus as claimed in claim 4, wherein said dedicated dummy register stores said inverse of  $X_i$  and said two shared dummy registers store said exclusive logical OR of  $X_i$  with  $Y_i$  and said inverse of the exclusive logical OR of  $X_i$  with  $Y_i$ .

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6. Apparatus as claimed in any one of claims 4 and 5, wherein said three further registers are provided for a subset of said plurality of data processing registers of said register bank.

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7. A method of processing data, said method comprising the steps of:

storing a data value in a data processing register; and

when said data value is stored in said data processing register also storing data values within three or more further registers such than a fixed relative number of bits within said data processing register and said three or more further registers as a whole transition from high to low and from low to high irrespective of what said data value is being written to data processing register and what data value was previously stored within said data processing register.

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8. A method as claimed in claim 7, wherein when writing a value  $X_i$  to an  $i^{\text{th}}$  bit of said data processing register previously storing a value of  $Y_i$ , also writing to corresponding bit positions within three further registers respective values of:

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an inverse of  $X_i$ ;

a new value  $Rd_i$  given by  $(\text{inverse}(X_i \text{ XOR } Y_i)) \text{ XOR } (\text{a value of } Rd_i \text{ currently stored});$  and

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an inverse of said new value of  $Rd_i$ .

9. A method as claimed in any one of claims 7 and 8, wherein said data processing register is one of a plurality of data processing registers of a register bank.

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10. A method as claimed in claim 8, wherein said three further registers comprise a dedicated dummy register dedicated to said data processing register and two shared dummy registers shared between said plurality of data processing registers of said register bank.

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11. A method as claimed in claim 10, wherein said dedicated dummy register stores said inverse of  $X_i$  and said two shared dummy registers store said exclusive logical OR of  $X_i$  with  $Y_i$  and said inverse of the exclusive logical OR of  $X_i$  with  $Y_i$ .

12. A method as claimed in any one of claims 10 and 11, wherein said three further registers are provided for a subset of said plurality of data processing registers of said register bank.